WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of first wiring structures of a first width which are arranged periodically at first intervals;

a second wiring structure which is formed next to one of the first wiring structures and the lower part of which has a second width substantially equal to the sum of n times the first width of the first wiring structure (n is a positive integer equal to two or more) and (n - 1) times the first interval.

2. The semiconductor device according to claim 1, wherein the upper part of the second wiring structure has n convex parts of substantially the first width and (n - 1) concave part.

3. The semiconductor device according to claim 2, wherein the (n - 1) concave part has a width substantially equal to the first interval.

4. The semiconductor device according to claim 2, wherein the second wiring structure are spaced from the one of the first wiring structures substantially at the first interval.

5. The semiconductor device according to claim 4, wherein the first and second wiring structures form a wiring structure in a memory cell array.

6. The semiconductor device according to claim 5, wherein the first wiring structures constitute memory

cells and the second wiring structure constitutes a select gate configured to select the memory cells.

7. The semiconductor device according to claim 6, wherein the first wiring structures constitute a memory cell unit of a NAND memory cell array.

8. The semiconductor device according to claim 7, wherein each of the first wiring structures comprises:

a first insulating film above a semiconductor substrate;

a first conductive film above the first insulating film;

a second insulating film above the first conductive film;

a second conductive film above the second insulating film; and

a third insulating film above the second conductive film.

9. The semiconductor device according to claim 7, wherein the second wiring structure comprises:

the first insulating film;

the first conductive film above the first insulating film;

the second conductive film above the first conductive film; and

the third insulating film above the second conductive film.

10. The semiconductor device according to claim 9,

wherein the second conductive film is formed in contact with the first conductive film in the second wiring structure.

11. The semiconductor device according to claim 10, wherein the second wiring structure further includes the second insulating film between the first conductive film and the second conductive film.

12. A semiconductor device manufacturing method comprising:

forming at least a first insulating film, a first conductive film, and a second insulating film above a semiconductor substrate sequentially;

forming a plurality of first resist patterns above the second insulating film periodically at first intervals, each of the first resist patterns having a first width corresponding to the width of a first wiring structure;

patterning at least the second insulating film by use of the first resist patterns to form a plurality of mask patterns, each of the mask patterns including the second insulating film;

selectively forming a second resist pattern in a space between the mask patterns in such a manner that the second resist pattern is formed in the space corresponding to a region where a second wiring structure wider than the first wiring structure is to be formed; and

patterning the first conductive film by use of the second resist pattern and the mask patterns.

13. The semiconductor device manufacturing method according to claim 12, further comprising:

forming a third insulating film on the first conductive film before the formation of the second insulating film in such a manner that the third insulating film is formed in a region excluding at least the region where the second wiring structure is to be formed; and

forming a second conductive film on the first conductive film and the third insulating film before the formation of the second insulating film.

14. A semiconductor device manufacturing method comprising:

forming at least a first insulating film, a first conductive film, and a second insulating film above a semiconductor substrate sequentially;

forming a first resist with a plurality of first patterns and a second pattern above the second insulating film, the first patterns being formed in a first region above the second insulating film and having almost the same width and interval as those of a plurality of first wiring structures and the second pattern being formed in a second region adjacent to the first region above the second insulating film and having a width substantially equal to the sum of

n times the width of a second wiring structure (n is a positive integer equal to two or more) and (n - 1) times the interval of the second wiring structures;

patterning the second insulating film and the first conductive film by use of the first resist to form the first wiring structures;

forming a second resist above the second insulating film in such a manner that the second resist is formed in a region excluding the space between the second wiring structures in the second region; and

patterning the second insulating film and the first conductive film by use of the second resist to form the second wiring structures.

15. The semiconductor device manufacturing method according to claim 14, further comprising:

forming a third insulating film in the first region excluding the second region on the first conductive film before the formation of the second insulating film; and

forming a second conductive film on the first conductive film and the third insulating film before the formation of the second insulating film.

16. A semiconductor device manufacturing method comprising:

forming at least a first insulating film, a first conductive film, and a second insulating film above a

semiconductor substrate sequentially;

selectively forming a third insulating film whose etching rate is lower than that of the second insulating film in a position corresponding to the region where a second wiring structure wider than a first wiring structure is to be formed;

forming a resist with a plurality of patterns above the second insulating film in the region where the first wiring structures are to be formed, each of the patterns having almost the same width and interval as those of the first wiring structures; and

patterning the second insulating film and the first conductive film by use of the resist and the third insulating film to form the first and second wiring structures.

17. The semiconductor device manufacturing method according to claim 16, wherein the third insulating film is formed inside the second insulating film.

18. The semiconductor device manufacturing method according to claim 16, wherein the third insulating film is formed on the second insulating film.

19. The semiconductor device manufacturing method according to claim 16, wherein the resist is also formed above the third insulating film.

20. The semiconductor device manufacturing method according to claim 16, further comprising:

forming a fourth insulating film in a region

excluding at least the region where the second wiring structure is to be formed on the first conductive film before the formation of the second insulating film; and

forming a second conductive film on the first conductive film and the fourth insulating film before the formation of the second insulating film.